CLAIMS

1. A stacked gate region of a memory cell comprising:

a field oxide region;

a tunnel oxide layer;

at least one floating gate layer formed over said tunnel oxide layer; and

at least one polysilicon wing formed adjacent to said at least one floating gate layer and over a portion of said field oxide region.

2. Said stacked gate region of claim 1, wherein said floating gate layer comprises a first deposited and patterned polysilicon layer.

3. The stacked gate region of claim 2, wherein said at least one polysilicon wing comprises a second deposited and patterned polysilicon layer.

4. The stacked gate region of claim 1, wherein said at least one poly silicon wing and said floating gate layer comprise polysilicon.

5. The stacked gate region of claim 1, wherein the at least one polysilicon wing is substantially vertical.

6. The stacked gate region of claim 1, wherein the at least one polysilicon wing is substantially co-planar with the floating gate layer.

7. The stacked gate region of claim 1, wherein the at least one polysilicon wing is adjacent a substantially vertical edge of the floating gate layer.

8. The stacked gate region of claim 1, wherein said at least one polysilicon wing is comprised of a first polysilicon and said at least one floating gate is comprised of a second polysilicon, wherein said second polysilicon is different than said first polysilicon.

9. A stacked gate region of a memory cell comprising:

a field oxide region;

a tunnel oxide layer;

at least one floating gate layer formed over said tunnel oxide layer; and

at least one ear formed adjacent to said at least one floating gate layer and over a portion of said field oxide region.

10. The stacked gate region of claim 9, wherein the field oxide region is formed in a trench.

11. The stacked gate region of claim 9, wherein the at least one ear is comprised of polysilicon.

12. A stacked gate region of a memory cell comprising:

a substrate having at least one semiconductor layer;

at least one trench formed in said substrate;

field oxide deposited in said at least one trench and extending above an upper surface of said substrate;

a tunnel oxide layer formed over at least a portion of said substrate;

at least one floating gate layer formed over said tunnel oxide layer; and

at least one polysilicon ear formed on said at least one floating gate layer and adjacent to said field oxide.

13. The stacked gate region of claim 12, wherein said at least one polysilicon ear is comprised of a first polysilicon and said at least one floating gate is comprised of a second polysilicon, wherein said second polysilicon is different than said first polysilicon.

14. A stacked gate region of a memory cell comprising:

a substrate having at least one semiconductor layer;

at least one trench formed in said substrate;

a tunnel oxide layer formed over at least a portion of said substrate;

at least one floating gate layer formed over said oxide layer;

field oxide deposited in said at least one trench; and

at least one polysilicon ear formed on said at least one floating gate layer.

15. The stacked gate region of claim 14, wherein said at least one polysilicon ear has only a lower edge in contact with said at least one floating gate layer.

16. The stacked gate region of claim 14, wherein said at least one polysilicon ear has a selected height corresponding to a desired capacitive coupling.

17. A stacked gate region of a memory cell comprising:

a substrate having at least one semiconductor layer;

a plurality of trenches formed in said substrate;

respective field oxide regions formed in said trenches;

a tunnel oxide layer formed over said substrate;

a floating gate layer formed over said tunnel oxide layer; and

a pair of polysilicon wings located adjacent to opposite ends of said floating gate layer, co-planer with said floating gate layer and over a portion of corresponding ones of said field oxide regions.

18. The stacked gate region of claim 17, wherein the floating gate layer comprises a plurality of floating gates and a corresponding pair of polysilicon wings for each of the plurality of floating gates.

19. A stacked gate region of a memory cell comprising:

a substrate having at least one semiconductor layer;

a plurality of trenches formed in said substrate;

respective field oxide regions formed in said trenches;

a tunnel oxide layer formed over said substrate;

a floating gate layer formed over said tunnel oxide layer; and

a pair of polysilicon ears formed adjacent to corresponding ones of said field oxide regions on said floating gate layer and projecting substantially perpendicular to an upper surface of the floating gate layer.

20. The stacked gate region of claim 19, wherein the floating gate layer comprises a plurality of floating gates and a corresponding pair of polysilicon wings for each of the plurality of floating gates.

21. A stacked gate region of a memory cell comprising:

a substrate having at least one semiconductor layer;

a plurality of trenches formed in said substrate;

respective field oxide regions formed in said trench;

a tunnel oxide layer formed over said substrate;

a floating gate layer formed over said tunnel oxide layer; and

a pair of polysilicon ears adjacent to a portion of said floating gate.

22. The stacked gate region of claim 21, wherein the floating gate layer comprises a plurality of floating gates and a corresponding pair of polysilicon wings for each of the plurality of floating gates.

23. A memory cell comprising:

a substrate having at least one semiconductor layer;

a source formed in said substrate;

a drain formed in said substrate;

at least one trench formed in said substrate;

a field oxide region formed in said trench;

a tunnel oxide layer formed over said substrate;

at least one floating gate layer formed over said tunnel oxide layer;

at least one polysilicon wing formed adjacent to said at least one floating gate layer and over a portion of said field oxide region;

a dielectric layer formed over said substrate and said floating gate layer; and

a control gate layer formed over said dielectric layer.

24. A memory cell comprising:

a substrate having at least one semiconductor layer;

at least one trench formed in said substrate;

a drain formed in said substrate;

a source formed in said substrate;

field oxide deposited in said at least one trench and extending above an upper surface of said substrate;

a tunnel oxide layer formed over at least a portion of said substrate;

at least one floating gate layer formed over said tunnel oxide layer;

at least one polysilicon ear formed on said at least one floating gate layer and adjacent to said field oxide;

a dielectric layer formed over said substrate and said floating gate layer; and

a control gate layer formed over said dielectric layer.

25. A memory cell comprising:

a substrate having at least one semiconductor layer;

at least one trench formed in said substrate;

a drain formed in said substrate;

a source formed in said substrate;

a tunnel oxide layer formed over at least a portion of said substrate;

at least one floating gate layer formed over said oxide layer;

field oxide deposited in said at least one trench;

at least one polysilicon ear formed on said at least one floating gate layer;

a dielectric layer formed over said substrate and said floating gate layer; and

a control gate layer formed over said dielectric layer.

26. A memory device comprising:

a source formed in a substrate;

a drain formed in the substrate;

a trench formed in the substrate;

a floating gate formed over the substrate; and

a wing formed over the substrate.

27. The memory device of claim 26, wherein the wing is comprised of polysilicon.

28. The memory device of claim 27, wherein the floating gate is a self aligned floating gate.

29. The memory device of claim 26, wherein the wing is substantially vertical.

30. The memory device of claim 26, wherein the wing is substantially co-planar with the floating gate.

31. The memory device of claim 26, wherein the wing is adjacent a substantially vertical edge of the floating gate.

32. The memory device of claim 26 further comprising:

field oxide formed in the trench, wherein the field oxide is at the a surface of the floating gate.

33. A memory device comprising:

a source formed in a substrate;

a drain formed in the substrate;

a floating gate formed over the substrate;

field oxide formed in substrate; and

an ear formed over the substrate.

34. The memory device of claim 33, wherein the ear is comprised of polysilicon.

35. The memory device of claim 33, wherein the ear is in proximity of, but not in contact with the field oxide.

36. The memory device of claim 33, wherein the ear extends substantially beyond bounds of the floating gate.

37. The memory device of claim 33, wherein vertical sides of the ear do not contact the floating gate.

38. The memory device of claim 33, wherein a vertical edge the ear is adjacent the field oxide and a bottom edge of the ear is adjacent the floating gate.

39. A memory device comprising:

a plurality of memory cells having a plurality of rows, each memory cell comprising:

a control gate, associated with a row, formed integral to a common word line associated with the row;

a source formed in a common region with a source of an adjacent memory cell;

a drain formed in another common region with a drain of an adjacent memory cell;

a floating gate; and

a pair of wings; and

a common source line formed from the common region of the plurality of memory cells; and

a conductive bit line connecting connected to the drain of each memory cell of the row.

40. A memory device comprising:

a plurality of memory cells having a plurality of rows, each memory cell comprising:

a control gate, associated with a row, formed integral to a common word line associated with the row;

a source formed in a common region with a source of an adjacent memory cell;

a drain formed in another common region with a drain of an adjacent memory cell;

a floating gate; and

a pair of ears; and

a common source line formed from the common region of the plurality of memory cells; and

a conductive bit line connecting connected to the drain of each memory cell of the row.

41. A method of fabricating a stacked gate region comprising:

providing a substrate having at least one semiconductor layer;

forming a tunnel oxide layer over said substrate;

forming a first polysilicon layer over said tunnel oxide layer;

forming a nitride layer over said first polysilicon layer;

masking selected areas of said first polysilicon layer;

etching unmasked areas of said first polysilicon layer leaving at least one floating gate layer;

patterning trench areas in the substrate;

depositing field oxide in said trench;

performing planarization to planarize a surface of said stacked gate region;

performing an oxide etch back to remove selected amounts of said field oxide;

removing said nitride layer; and

depositing a second polysilicon layer over said substrate and removing selected portions of said second polysilicon layer so as to leave polysilicon wings formed adjacent to said at least one floating gate layer and over a portion of said field oxide.

42. The method of claim 41, wherein said selected portions of said second polysilicon layer are removed by performing a spacer etch of selected portions of said second polysilicon layer.

43. The method of claim 41, wherein selected amounts of said field oxide are removed by performing an oxide etch back to remove selected amounts of said field oxide such that said field oxide is below an upper surface of said at least one floating gate layer.

44. The method of claim 41, wherein planarization is performed through mechanical planarization.

45. The method of claim 41, wherein masking said selected areas further comprises depositing a layer of photo resist and the method further comprises removing said layer of photo resist prior to depositing said field oxide.

46. The method of claim 41, wherein said trench areas are patterned by masking selected areas of said stacked gate region and etching said tunnel oxide layer, said nitride layer and said substrate to a desired depth in unselected areas of said stacked gate region.

47. The method of claim 41, wherein selected areas of said first polysilicon layer are masked by depositing photo resist on said selected areas.

48. A method of fabricating a stacked gate region comprising:

providing a substrate having at least one semiconductor layer;

forming a tunnel oxide layer over said substrate;

forming a first polysilicon layer over said tunnel oxide layer;

forming a nitride layer over said first polysilicon layer;

etching said layers to produce at least one floating gate layer;

forming field oxide regions in the substrate;

performing planarization to planarize a surface of said stacked gate region;

removing a portion of said field oxide;

removing said nitride layer; and

forming wings.

49. The method of claim 48, wherein forming wings comprises depositing a second polysilicon layer over said substrate and

removing selected portions of said second polysilicon layer so as to leave polysilicon wings formed adjacent to said at least one floating gate layer and over a portion of said field oxide.

50. The method of claim 48, wherein forming field oxide regions in the substrate comprises patterning trench areas in the substrate and depositing field oxide in said trench areas.

51. The method of claim 48, wherein removing a portion of said field oxide comprises performing an oxide etch back to remove selected amounts of said field oxide.

52. The method of claim 48, wherein etching said layers to produce at least one floating gate layer comprises masking selected areas of said first polysilicon layer and etching unmasked areas of said first polysilicon layer leaving at least one floating gate layer.

53. A method of fabricating a stacked gate region comprising:

providing a substrate having at least one semiconductor layer;

forming a tunnel oxide layer over said substrate;

forming a first polysilicon layer over said tunnel oxide layer;

forming a nitride layer over said first polysilicon layer;

selectively removing areas of said nitride layer and first polysilicon layer leaving at least one floating gate layer;

patterning trench areas in the substrate;

depositing field oxide in said trench areas;

planarizing a surface of said stacked gate region;

removing said nitride layer;

depositing a second polysilicon layer over said substrate;

selectively removing portions of said second polysilicon layer leaving single sided ears, each having one vertical side adjacent to sides of said field oxide and one lower side on one of said at least one floating gate layer.

54. The method of claim 53, wherein said nitride layer is removed by selectively etching remaining portions of said nitride layer.

55. The method of claim 53, wherein said trench areas are patterned by masking selected areas of said stacked gate region and etching said tunnel oxide layer, said nitride layer and said

substrate to a desired depth in unselected areas of said stacked gate region.

56. The method of claim 53, wherein surfaces of said stacked gate region are planarized by performing mechanical planarization on said field oxide and nitride layers.

57. The method of claim 53, wherein said areas of said nitride layer and said first polysilicon layer are selectively removed by masking selected areas and etching said nitride layer and first polysilicon layer in unselected areas leaving at least one floating gate layer in said selected areas.

58. A method of fabricating a stacked gate region comprising:

providing a substrate having at least one semiconductor layer;

forming a tunnel oxide layer over said substrate;

forming a first polysilicon layer over said substrate;

forming a nitride layer over said first polysilicon layer;

removing selected portions of said tunnel oxide layer, said first polysilicon layer, said nitride layer and said substrate to form at least one shallow trench to a desired depth;

depositing field oxide into said at least one shallow trench;

planarizing said field oxide and said nitride layer to create a planar surface of said stacked gate region;

removing said nitride layer;

depositing a second polysilicon layer over said substrate and selectively removing portions of said second polysilicon layer leaving single sided ears, each having one vertical side adjacent to sides of said field oxide and one lower side on one of said at least one floating gate layer; and

removing a portion of said field oxide such that an upper surface of said field oxide is substantially co-planer with an upper surface of said at least one floating gate layer leaving double sided ears.

59. The method of claim 58, wherein said field oxide and said nitride layer are planarized by performing chemical mechanical planarization on said field oxide and said nitride layer.

60. The method of claim 58, wherein said substrate comprises silicon.

61. A method of fabricating a memory cell comprising:

providing a substrate having at least one semiconductor layer;

forming a floating gate layer over said substrate;

forming a trench in said substrate; and

forming a polysilicon wing adjacent to a vertical edge of said floating gate.

62. The method of claim 61 further comprising depositing field oxide into said shallow trench.

63. The method of claim 61, wherein forming a trench is performed by a shallow trench isolation etch instead of photolithography.

64. A method of fabricating a memory cell comprising:

providing a substrate having at least one semiconductor layer;

forming a floating gate layer over said substrate without using floating gate layer photolithography;

forming a shallow trench in said substrate;

depositing field oxide into said shallow trench beyond an upper surface of said floating gate layer; and

forming a polysilicon ear over said floating gate layer and adjacent to an exposed vertical edge of said field oxide.

65. The method of claim 64, wherein forming a polysilicon ear comprises forming a polysilicon ear to a desired height corresponding to a desired capacitive coupling of said memory cell.

66. A method of fabricating a memory cell comprising:

providing a substrate having at least one semiconductor layer;

forming a floating gate layer over said substrate without using floating gate layer photolithography;

forming a shallow trench in said substrate;

depositing field oxide into said shallow trench beyond an upper surface of said floating gate layer;

forming a polysilicon ear over said floating gate layer and adjacent to an exposed vertical edge of said field oxide; and

removing field oxide such that an upper surface of said field oxide is substantially planar to said upper surface of said floating gate layer.

67. A method of fabricating a memory cell comprising:

providing a substrate having at least one semiconductor layer;

forming a source and drain in said substrate;

forming a tunnel oxide layer over said substrate;

forming a first polysilicon layer over said tunnel oxide layer;

forming a nitride layer over said first polysilicon layer;

masking selected areas of said first polysilicon layer;

etching unmasked areas of said first polysilicon layer leaving at least one floating gate layer;

patterning trench areas in the substrate;

depositing field oxide in said trench;

performing planarization to planarize a surface of said stacked gate region;

performing an oxide etch back to remove selected amounts of said field oxide;

removing said nitride layer;

depositing a second polysilicon layer over said substrate and removing selected portions of said second polysilicon layer so as to leave polysilicon wings formed adjacent to said at least one floating gate layer and over a portion of said field oxide;

forming a dielectric layer over said floating gate layer, said polysilicon wings and said substrate; and

forming a control gate layer over said dielectric layer.

68. A method of fabricating a memory cell comprising:

providing a substrate having at least one semiconductor layer;

forming a source and a drain in said substrate;

forming a tunnel oxide layer over said substrate;

forming a first polysilicon layer over said tunnel oxide layer;

forming a nitride layer over said first polysilicon layer;

selectively removing areas of said nitride layer and first polysilicon layer leaving at least one floating gate layer;

patterning trench areas in the substrate;

depositing field oxide in said trench areas;

planarizing a surface of said stacked gate region;

removing said nitride layer;

depositing a second polysilicon layer over said substrate;

selectively removing portions of said second polysilicon layer leaving single sided ears, each having one vertical side adjacent to sides of said field oxide and one lower side on one of said at least one floating gate layer;

forming a dielectric layer over said floating gate layer, said polysilicon wings and said substrate; and

forming a control gate layer over said dielectric layer.

69. A method of fabricating a memory cell comprising:

providing a substrate having at least one semiconductor layer;

forming a source and a drain in said substrate;

forming a tunnel oxide layer over said substrate;

forming a first polysilicon layer over said substrate;

forming a nitride layer over said first polysilicon layer;

removing selected portions of said tunnel oxide layer, said first polysilicon layer, said nitride layer and said substrate to form at least one shallow trench to a desired depth;

depositing field oxide into said at least one shallow trench;

planarizing said field oxide and said nitride layer to create a planar surface of said stacked gate region;

removing said nitride layer;

depositing a second polysilicon layer over said substrate and selectively removing portions of said second polysilicon layer leaving single sided ears, each having one vertical side

adjacent to sides of said field oxide and one lower side on one of said at least one floating gate layer;

removing a portion of said field oxide such that an upper surface of said field oxide is substantially co-planer with an upper surface of said at least one floating gate layer leaving double sided ears;

forming a dielectric layer over said floating gate layer, said polysilicon wings and said substrate; and

forming a control gate layer over said dielectric layer.

70. A method of fabricating a stacked gate region comprising:

forming a floating gate;

forming a region with a surface lower than the surface of the floating gate; and

forming at least one wing connected to the region and the floating gate.

71. A method of fabricating a stacked gate region comprising:

forming a floating gate;

forming a region with a surface lower than the surface of the floating gate; and

forming at least one ear connected to the region and the floating gate.

72. A computer system comprising:

at least one processor;

a system bus; and

a memory device coupled to said system bus, said memory device including one or more memory cells, each memory cell including at least one stacked gate region comprising:

a substrate having at least one semiconductor layer;

a shallow trench isolation area;

an oxide layer formed over said substrate and said shallow trench isolation area;

a floating gate layer formed over said oxide layer; and

at least one polysilicon wing formed adjacent to vertical edges of said floating gate layer and over said oxide layer.